



PJ1870

20V Common-Drain Dual N-Channel MOSFET-ESD Protected

FEATURES

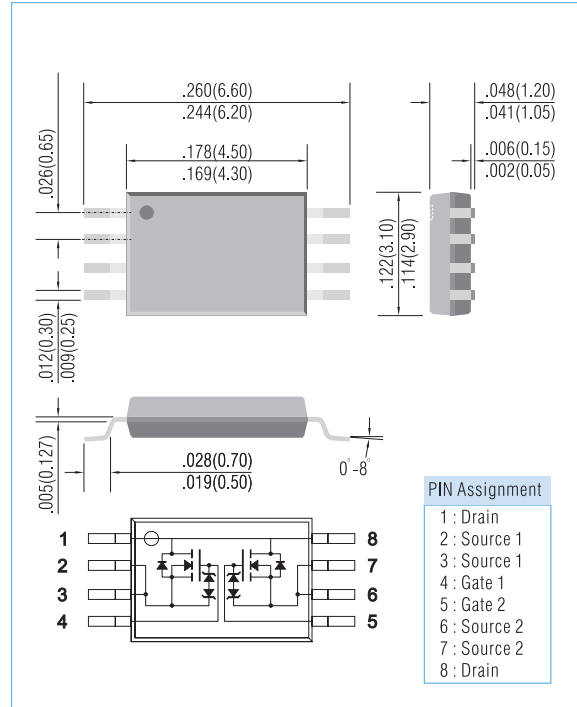
- $R_{DS(ON)}$, V_{GS} @4.5V, I_{DS} @6.5A=19m Ω
- $R_{DS(ON)}$, V_{GS} @3.5V, I_{DS} @6.0A=21m Ω
- $R_{DS(ON)}$, V_{GS} @2.5V, I_{DS} @5.5A=27m Ω
- Advanced trench process technology
- High Density Cell Design For Ultra Low On-Resistance
- Specially Designed for Li-Ion or Li-Polymer battery packs
- ESD Protected 1.5KV HBM
- Pb free product : 99% Sn above can meet RoHS environment substance directive request

MECHANICAL DATA

- Case: TSSOP-8 plastic case.
- Terminals : Solderable per MIL-STD-750, Method 2026
- Marking : 1870

TSSOP-8

Unit: inch (mm)



Maximum RATINGS and Thermal Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 12	V
Continuous Drain Current	I _D	6	A
Pulsed Drain Current ¹⁾	I _{DM}	30	A
Maximum Power Dissipation	P _D	1.5 0.9	W
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 to 150	°C
Junction-to-Ambient Thermal Resistance (PCB mounted) ²⁾	R _{θJA}	83	°C/W

- Note: 1. Maximum DC current limited by the package
2. Surface mounted on FR4 board, t ≤ 10 sec

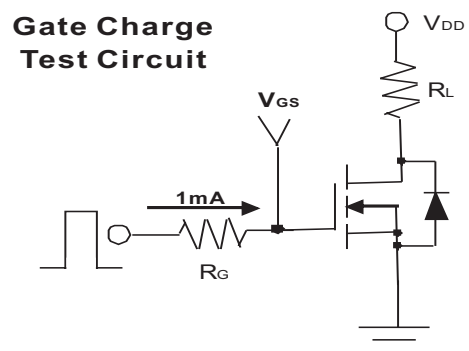
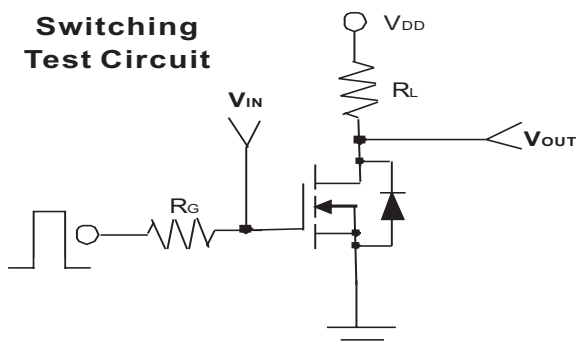
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ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.5	-	-	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 6.5A$	-	15	19	mΩ
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 3.5V, I_D = 6.0A$	-	17	21	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 2.5V, I_D = 5.5A$	-	21	27	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20V, V_{GS} = 0V$	-	-	1	μA
Gate Body Leakage	I_{GSS}	$V_{GS} = \pm 12V, V_{DS} = 0V$	-	-	± 10	μA
Dynamic						
Total Gate Charge	Q_g	$V_{DS} = 10V, I_D = 6.5A, V_{GS} = 5V$	-	22.0	-	nC
			-	42.5	-	
Gate-Source Charge	Q_{gs}	$V_{DS} = 10V, I_D = 6.5A, V_{GS} = 10V$	-	2.5	-	ns
Gate-Drain Charge	Q_{gd}		-	4.7	-	
Turn-On Delay Time	$T_{d(on)}$		-	18	23	
Turn-On Rise Time	t_{rr}	$V_{DD} = 10V, R_L = 10\Omega, I_D = 1A, V_{GEN} = 4.5V, R_G = 3.6\Omega$	-	28	40	ns
Turn-Off Delay Time	$t_{d(off)}$		-	140	195	
Turn-Off Fall Time	t_f		-	30	42	
Input Capacitance	C_{iss}	$V_{DS} = 10V, V_{GS} = 0V, f = 1.0\text{ MHz}$	-	1450	-	pF
Output Capacitance	C_{oss}		-	210	-	
Reverse Transfer Capacitance	C_{rss}		-	155	-	
Source-Drain Diode						
Max. Diode Forward Current	I_S	-	-	-	1.5	A
Diode Forward Voltage	V_{SD}	$I_S = 1.5A, V_{GS} = 0V$	-	0.64	1.2	V





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Typical Characteristics Curves ($T_A=25^\circ\text{C}$, unless otherwise noted)

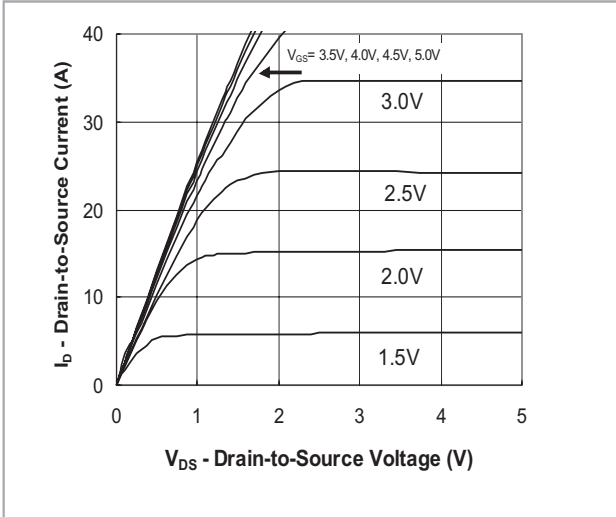


FIG.1- Output Characteristic

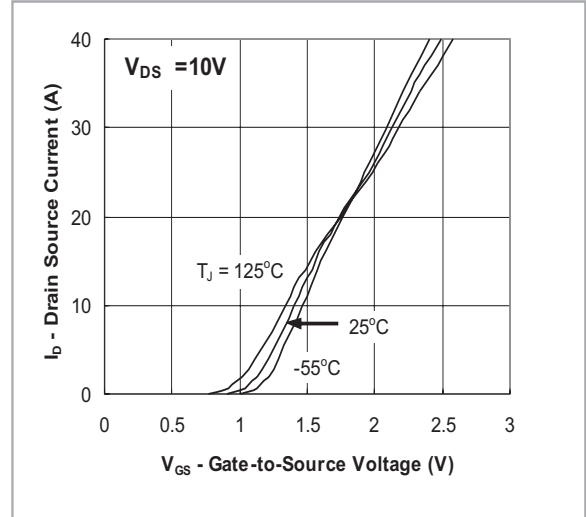


FIG.2- Transfer Characteristic

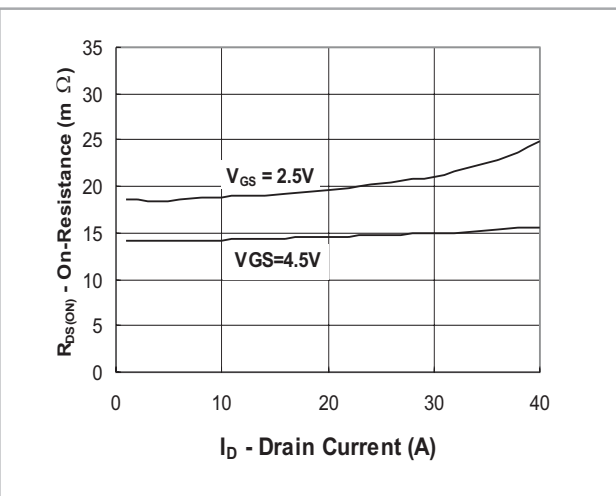


FIG.3- On Resistance vs Drain Current

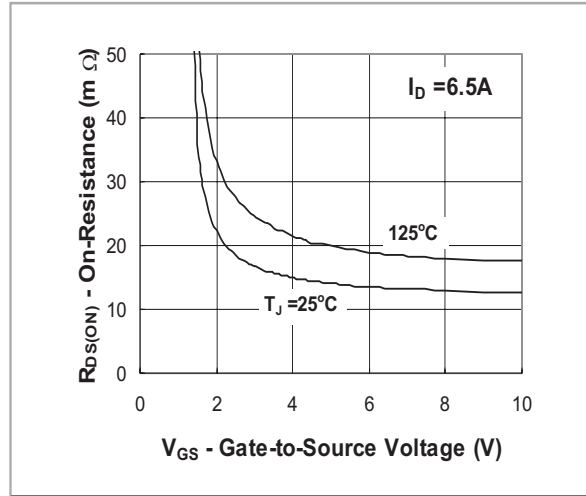


FIG.4- On Resistance vs Gate to Source Voltage

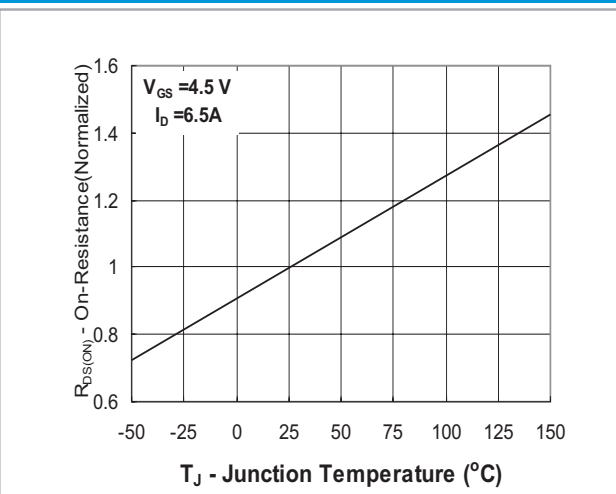


FIG.5- On Resistance vs Junction Temperature

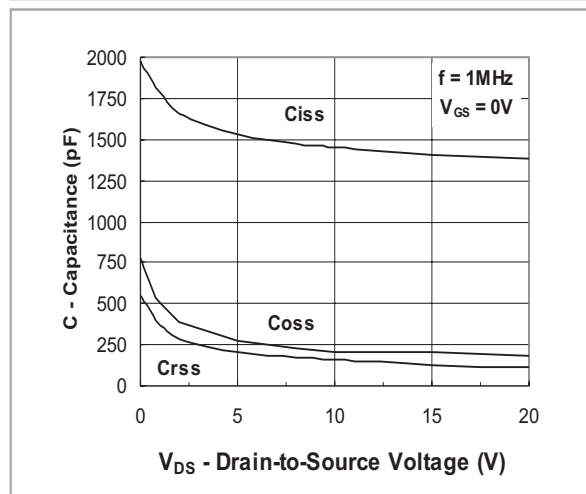


FIG.6- Capacitance



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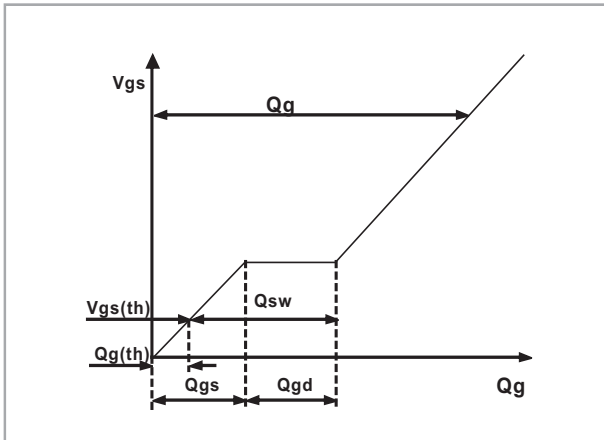


Fig.7 - Gate Charge Waveform

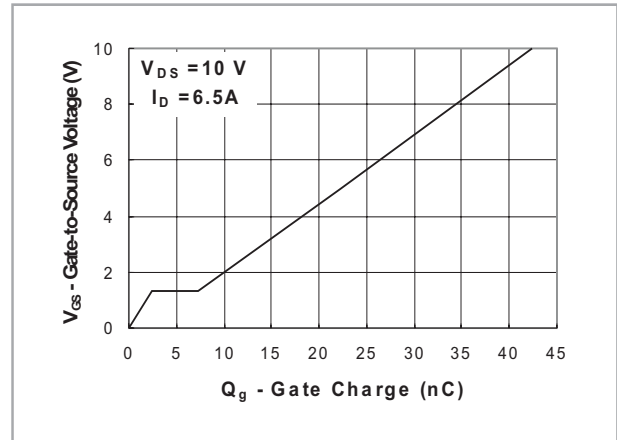


Fig.8 - Gate Charge

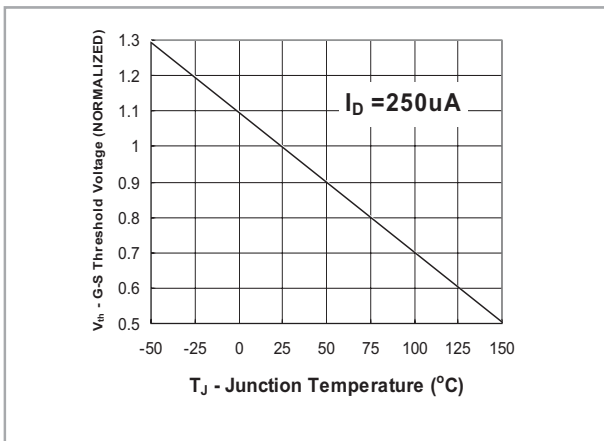


Fig.9 - Threshold Voltage vs Temperature

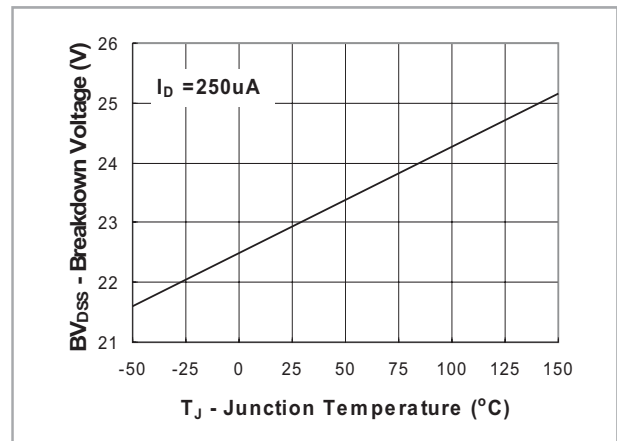


Fig.10 - Breakdown Voltage vs Junction Temperature

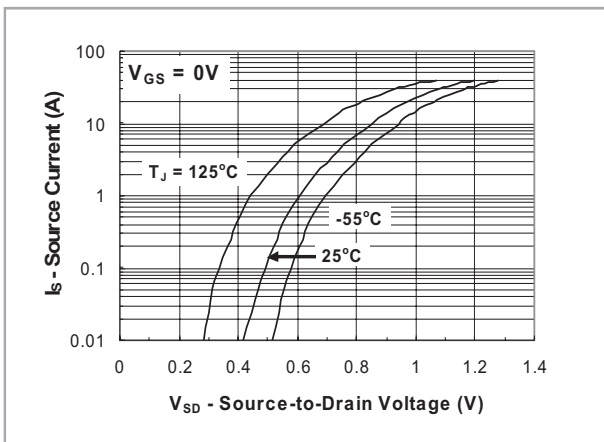
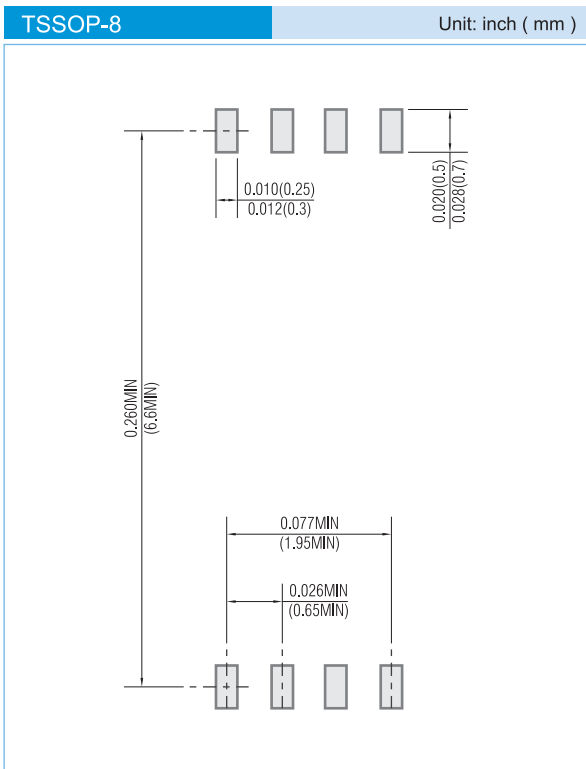


Fig.11 - Source-Drain Diode Forward Voltage



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MOUNTING PAD LAYOUT



ORDER INFORMATION

- Packing information
T/R - 3K per 13" plastic Reel

LEGAL STATEMENT

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